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(54) **Digital-to-analog converter deglitching circuit**

(57) A circuit for eliminating undesired electrical transients associated with digital-to-analog converters delays the output of the converter by an amount of time slightly greater than the width of a typical glitch. The circuit output is then switched between the undelayed and delayed outputs according to a switch control signal at the same frequency as the sample clock frequency. Unclocked operation is also possible.

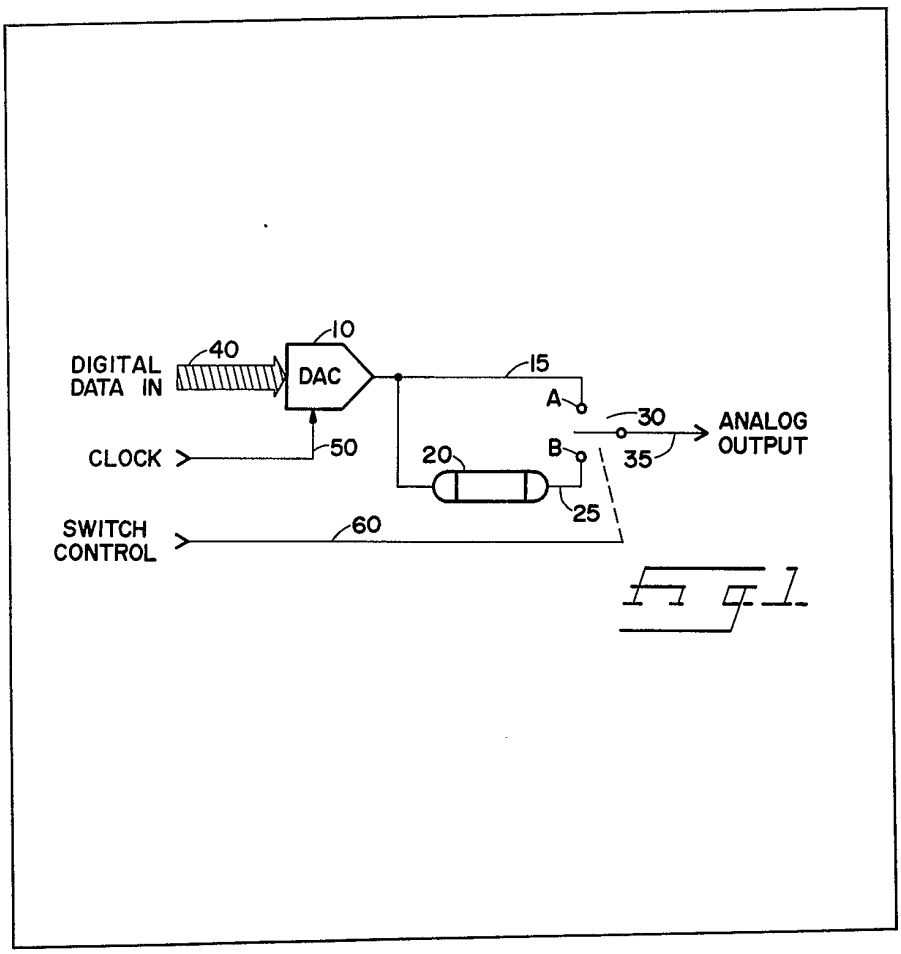

Fig 1

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The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

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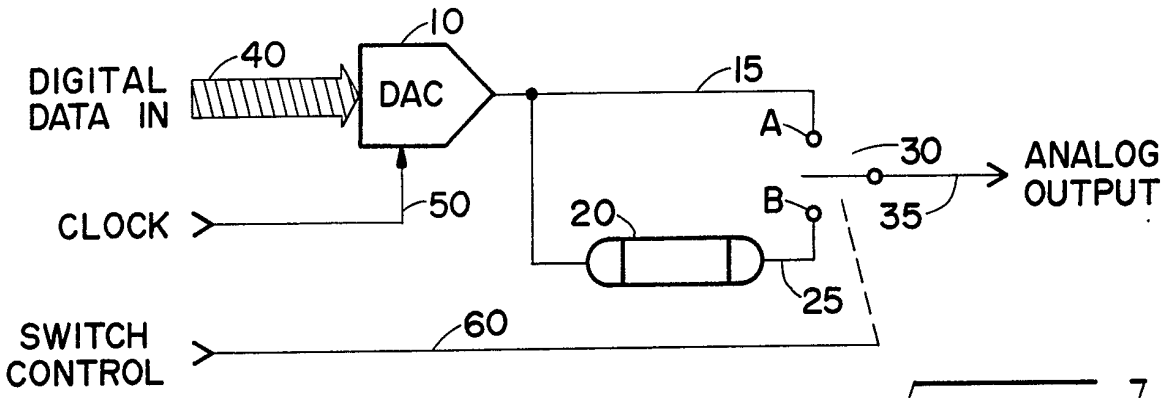

Fig 1

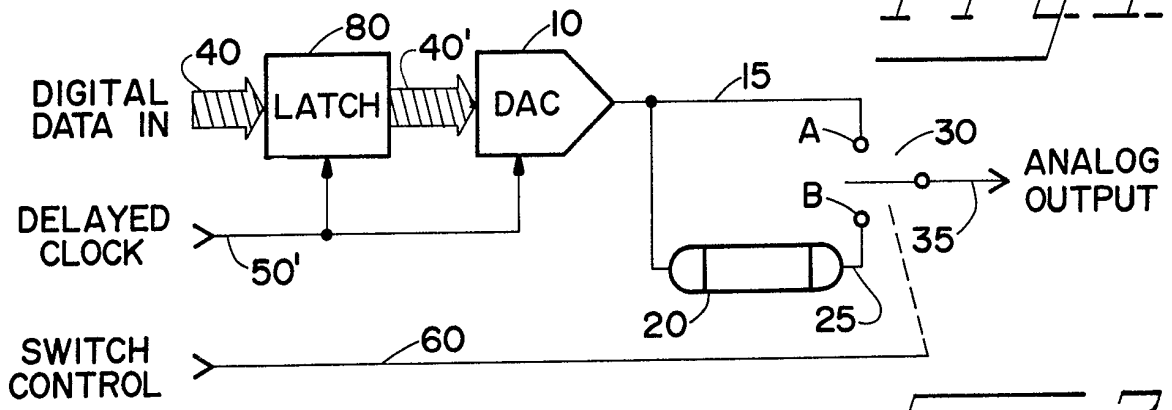

Fig 2

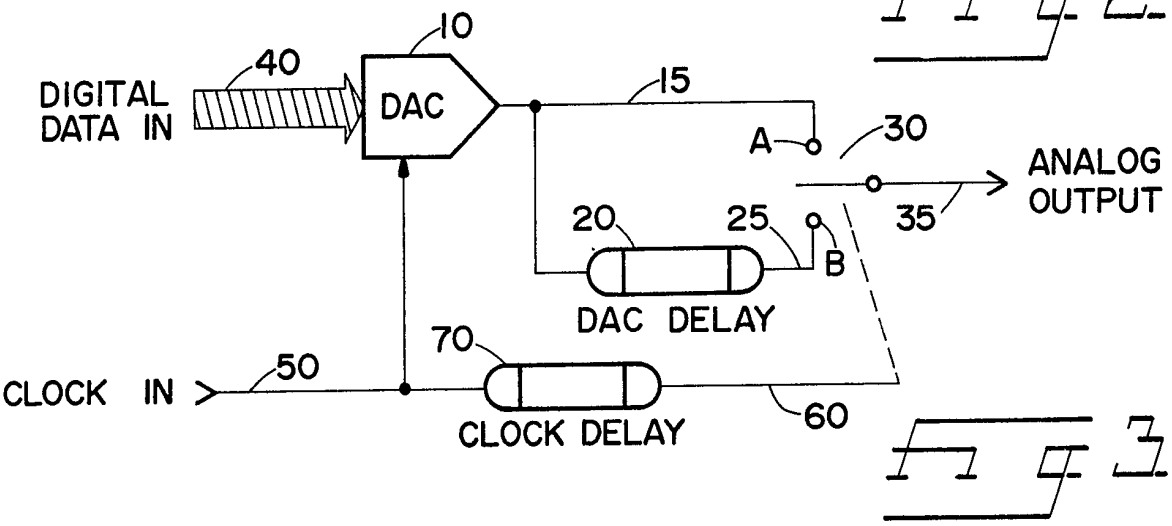

Fig 3

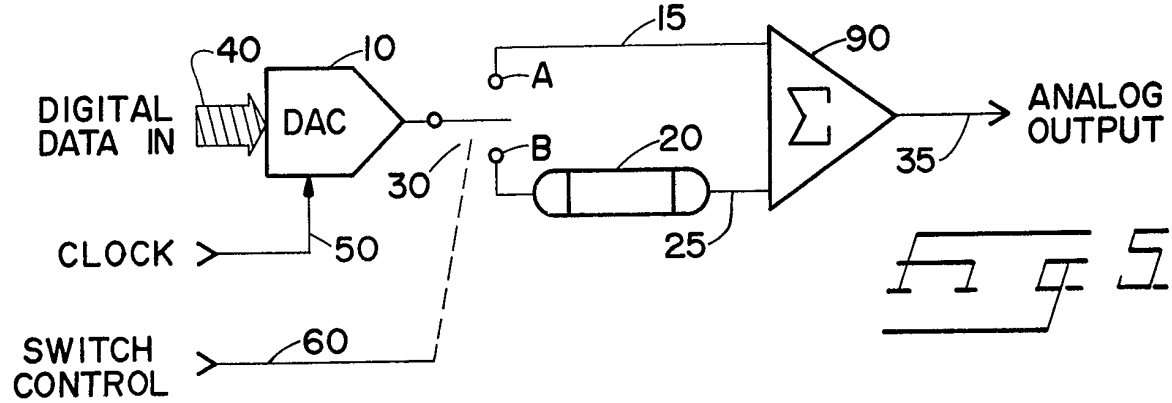

Fig 5

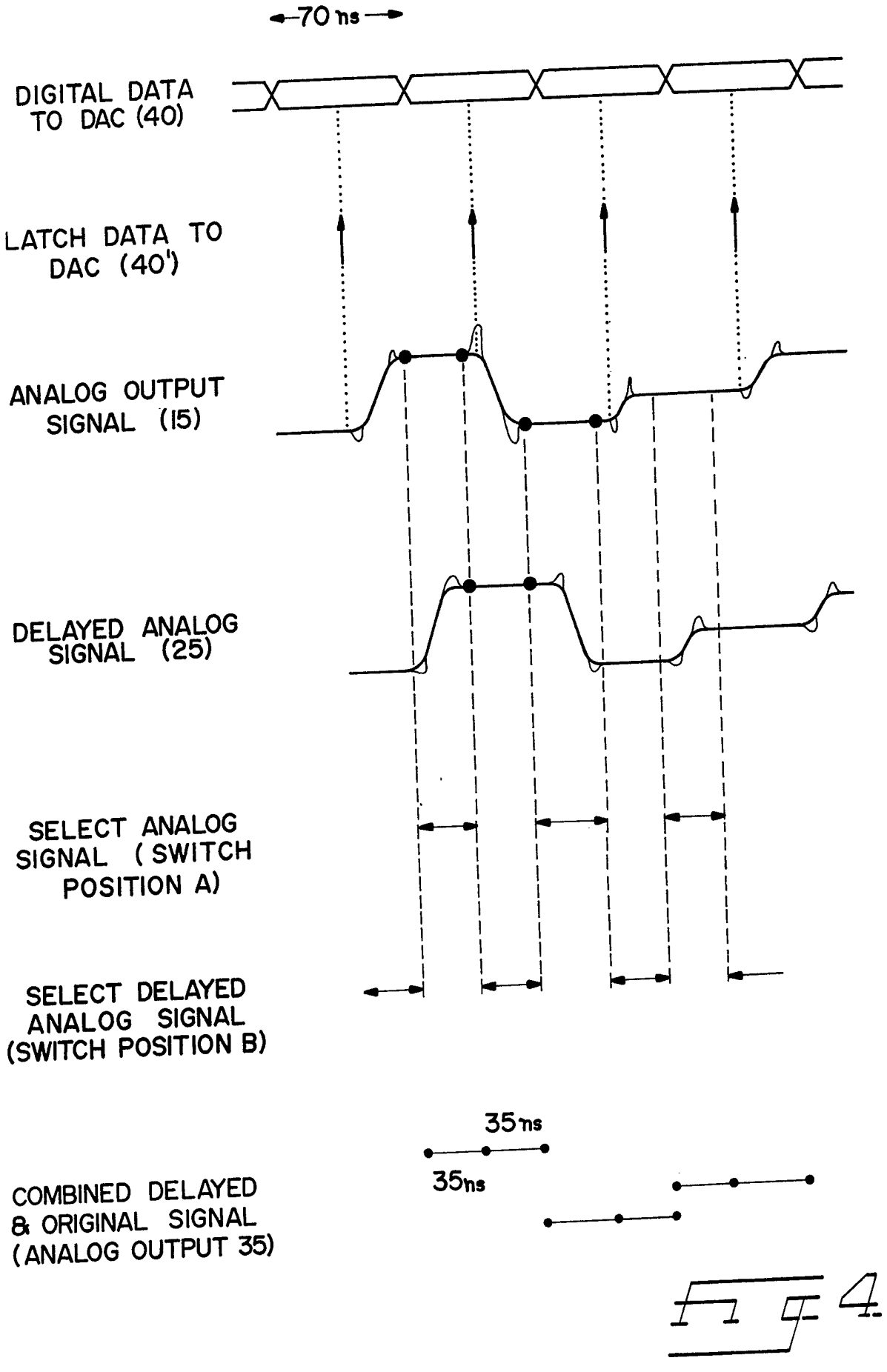
70 ns
DIGITAL DATA TO DAC (40)
LATCH DATA TO DAC (40')
ANALOG OUTPUT SIGNAL (15)
DELAYED ANALOG SIGNAL (25)
SELECT ANALOG SIGNAL (SWITCH POSITION A)
SELECT DELAYED ANALOG SIGNAL (SWITCH POSITION B)
35 ns
35ns
COMBINED DELAYED & ORIGINAL SIGNAL (ANALOG OUTPUT 35)

Fig 4

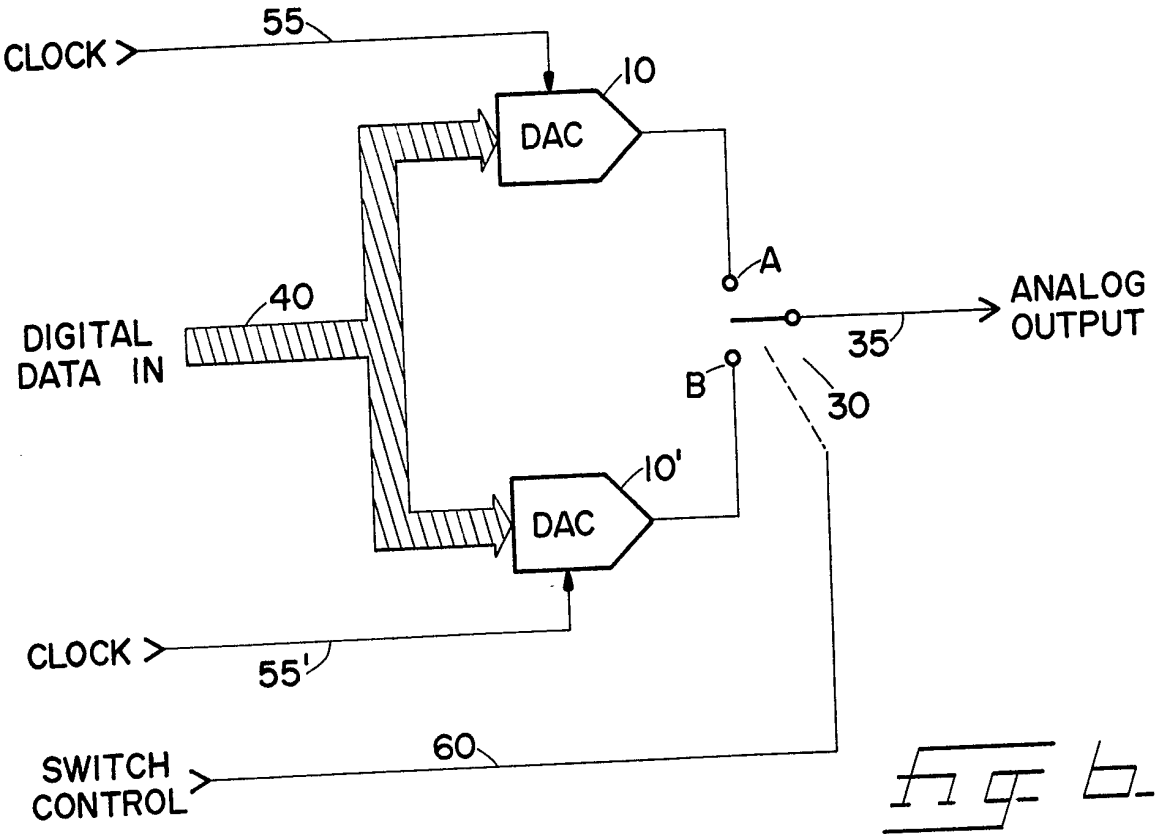
CLOCK
55
10
DAC
A
ANALOG
OUTPUT
40
DIGITAL
DATA IN
35
B
30
10'
DAC
CLOCK
55'
SWITCH
CONTROL
60

Fig 6

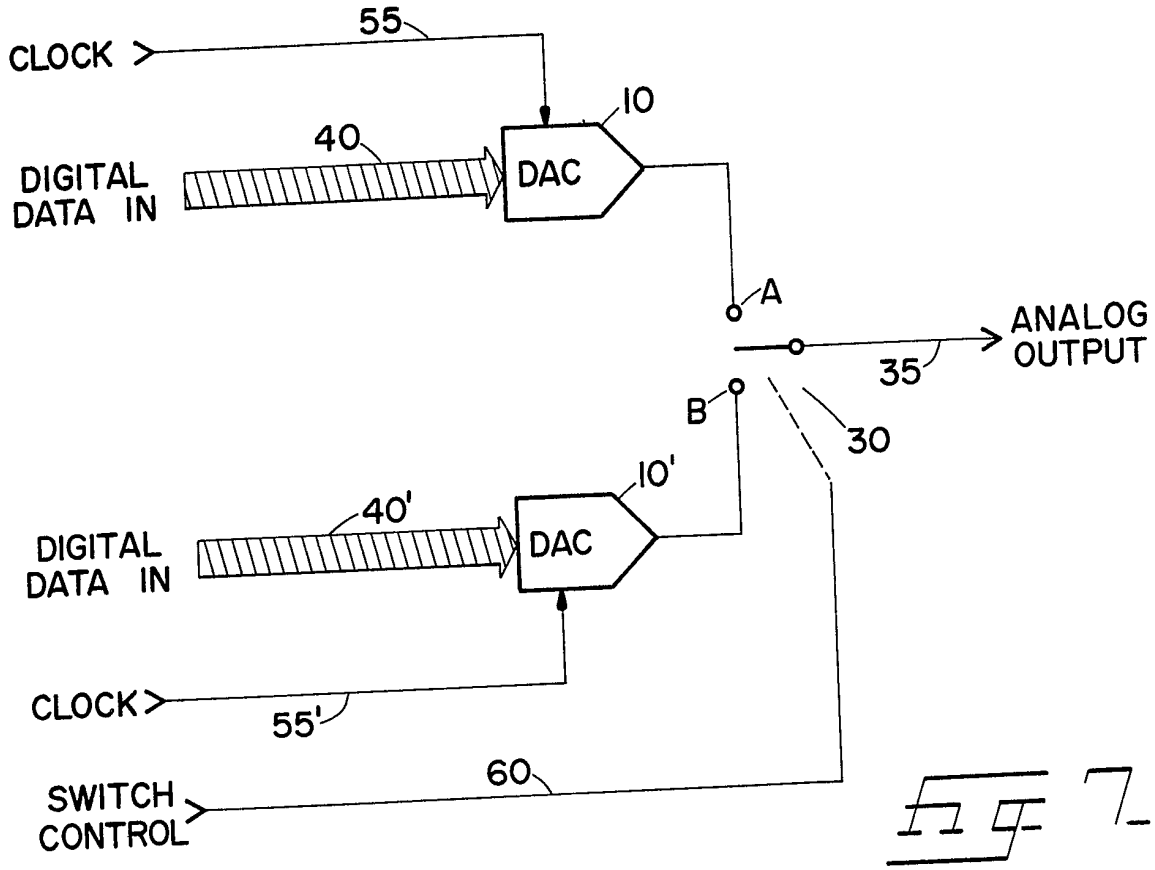
CLOCK
55
10
40
DIGITAL
DATA IN
DAC
A
ANALOG
OUTPUT
35
B
30
10'
40'
DIGITAL
DATA IN
DAC
CLOCK
55'
SWITCH
CONTROL
60

Fig 7

SPECIFICATION

Digital-to-analog converter deglitching circuit

Background of the invention

This invention pertains to digital-to-analog converters and more particularly to an apparatus for removing undesirable signal transients or glitches from the output of a digital-to-analog converter.

All simple digital-to-analog converters, hereinafter referred to as DAC's, have inherent limitations that cause troublesome signal transients or glitches. These glitches are analog signal spikes appearing at the DAC's output immediately following a transition of the DAC's input logic code.

These glitches are usually caused by switch imperfections, notably the difference in turn on and turn off times of the DAC's current steering transistors. If, for example, the DAC's switching transistors are faster switching off than switching on, then one would find that when changing the DAC's logic input from 011 ... 11 to 100 ... 00 an intermediate code of 00 ... 00 may be produced. In this situation, all bits are momentarily off and the output level (for a positive output DAC) initially heads towards zero instead of +1/2 full scale. The resultant spike occurring before the DAC settles at +1/2 full scale is known as a glitch.

In high-speed automatic test equipment, process control systems and interactive displays, glitches from DAC's can cause such problems as damage to components under test, overloading of the sensing circuits or even averaged errors in high-inertia electrical and mechanical systems. In video applications, glitches can cause differential gain and phase errors.

Various methods have been devised for lessening the impact of glitches. For example, are slew rate limiters or nonlinear filters such as that disclosed in U.S. Patent No. 4,163,948 Filter For Digital-To-Analog Converter, issued to M.L. Rieger and M.D. Singer and U. Guadagno and G.V. Pallottino, *Nonlinear filters for noise rejection with application to deglitching,* Alta Frequenze, v. 46, No. 9, September 1977, pp. 416-421. These filters only provide useful performance for rejecting glitches on signals of known slew rate and are, therefore, not useful for arbitrary signals.

Other techniques such as that described in the article "High-speed Analogue-to-digital Conversion" by O.J. Dowing and P.T. Johnson, Wireless World, December 1977, pp. 65-70, involve resampling the DAC output, using a delayed clock, after the glitches have settled. This technique, however, causes current transients in the storage element because the output data must be transferred almost instaneously to the hold capacitor. Another deglitching method is to pass the DAC output through a conventional low pass linear filter. This technique merely redistributes the glitch energy and does not eliminate it.

Summary of the invention

The present invention overcomes the above-described problems associated with attenuating glitches by delaying the DAC output by an amount of time slightly greater than the width of a typical glitch. The output of the circuit then is switched between the undelayed DAC output and the delayed DAC output according to a switch control signal at the same frequency as the sample clock frequency.

It is therefore an object of the present invention to provide a DAC deglitcher which overcomes the disadvantages of the prior art.

It is another object of the present invention to provide a DAC deglitching circuit which does not develop current or voltage transients in the storage element.

It is yet another object of the present invention to provide a DAC deglitcher that removes all the glitch energy.

The foregoing and numerous other objects, advatages and inherent functions of the present invention will become apparent as the same is more fully understood from the following description. It is to be understood, however, that the embodiment described is not intended to be exhausing nor limiting of the invention and is presented as an example only.

Brief description of the drawings

In the drawings:

Figure 1 is a block diagram of a preferred embodiment of the present invention;

Figure 2 is a block diagram of another preferred embodiment of the present invention;

Figure 3 is a block diagram of yet another preferred embodiment of the present invention;

Figure 4 contains waveforms which will be helpful in understanding the embodiments of Figure 1, 2, and 3;

Figure 5 is a block diagram of an alternative embodiment of the present invention;

Figure 6 is a block diagram of another alternative embodiment of the present invention; and

Figure 7 depicts a variation of Figure 6.

Detailed description of the preferred embodiment

Referring to Figure 1 and Figure 4, in accordance with the present invention, a digital-to-analog converter DAC 10, as known from the prior art receives digital data 40 as an input. DAC 10 represents a typical DAC for translating or converting the digital word input signal to an analog waveform. As DAC 10 is of conventional design, no detailed discussion thereof is believed necessary. However, for those who desire more information on digital-to-analog converters, see *Integrated Electronics Analog and Digital Circuits and Systems* by Millman and Halkias, copyright 1972 by McGraw-Hill, Inc.

The output of DAC 10 may be the analog output signal designated 15 in Figure 4. This DAC output signal contains glitches whenever the input digital word 40 is changed. The glitches are normally caused by unequal propogation delays among the bits arriving at the DAC input or by variations in the transient response of the binary weighted elements within the DAC or a combination of both. DAC 10 is clocked in the conventional manner by a sampling clock signal 50. Or alternatively DAC 10 may be unclocked.

The output of DAC 10 is routed in two directions:

directly to terminal A of switch 30 and to the B terminal of switch 30 via delay 20. Switch 30 may be any conventional analog switching means capable of being switched by an external control signal 60. Switch control signal 60 is alternates at the same frequency as sampling clock signal 50. It is, however, not necessarily of the same phase or duty cycle as sampling clock signal 50. Delay 20 is a conventional delay line and may provide approximately 30 nanoseconds of delay in a typical application wherein the date conversion is occurring at a rate of 14 MHz and the expected width of a glitch is approximately 10-20 nanoseconds. Therefore, the amount delay provided by delay 20 is slightly greater than the expected glitch width.

By way of operation then, the digital signal 40 enters DAC 10 wherein it is converted to an analog output signal in the conventional manner. Switch 30 then switches either analog output signal 15 or delayed signal 25 to the output. The duty cycle of switch control signal 60 is such that analog output signal 15 is only switched to the output after any possible glitch has settled. The same is true for delayed analog signal 25. Thus, the composite analog output signal 35 is comprised of only the glitch free portions of the delayed and non-delayed output of DAC 10. The duty cycle of switch control signal may typically be 50 percent.

Figure 2 is illustrative of an embodiment of the present invention wherein a latch circuit 80 is operably connected between the input data 40 and DAC 10. In operation the addition of latch circuit 80 serves to limit data propagation error with a delayed sampling clock 50'.

The embodiment of Figure 3 illustrates the concept that switch control signal 60 may be a delayed version of sample clock 50. The operation of this embodiment is identical to that shown in Figure 1 and merely illustrates a convenient manner of deriving the switch control signal.

Figure 5 illustrates another embodiment of the present invention wherein the switching takes place before the output of DAC 10 is delayed. A summing amplifier 90 has been added in order to sum the output of DAC 10 with the delayed output of DAC 10 to produce deglitched output 35.

An extension of the above-decribed technique is shown in Figure 6. The circuit of Figure 6 utilizes a plurality of DAC's rather than the single DAC of the previous embodiments. Each of the DAC's receive the same input digital data 40 but at different times. This is accomplished by clocking the DAC's with different phases of the clock signal. The embodiment of Figure 6 depicts DAC 10 being clock by clock phase 55 and DAC 10' being clocked by clock phase 55'. Switch 30 is then used in the previously described manner to alternatively select the output of each DAC such that the glitches are avoided.

Figure 7 is a variation of the technique of Figure 6. The embodiment of Figure 7 utilizes a plurality of DAC's clocked by different clock phases but the input digital data 40 and 40' is received sequentially (alternatively) not simultaneously. Since the DAC's are clocked on different clock phases, their analog output change at different points in time. Switch 30 and control signal 60 are then utilized as before to alternately select the output of each DAC in order to avoid the glitches.

From the foregoing it will be seen that the applicants have provided a new and novel method for deglitching the output of a digital-to-analog converter. However, it may be observed that the foregoing specification has not been burdened by the inclusion of large amounts of detail concerning specific circuitry since such matters are considered to be within the skill of the art. It should be noted that the particular embodiments which are shown and described herein are intended to be illustrative and not restrictive of the invention. Therefore, the appended claims are intended to cover all modifications which fall within the scope of the foregoing specification.

CLAIMS

1.A deglitching circuit for use with a digital-to-analog convertor for converting a digital signal to an analog signal comprising:

delay means coupled to receive the output of the digital-to-analog converter, said delay means having a delay slightly greater than the width of a typical glitch;

switching means having two input terminals, one output terminal, and a control terminal, the output of said delay means being connected to one of said input terminals and the output of the digital-to-analog converter being connected to the other one of said input terminals, said control terminal being driven by a switch control signal such that glitches present on either the output of the digital-to-analog converter or the output of said delay means are not transmitted to said output terminal.

2. The deglitching circuit according to claim 1 wherein said switch control signal is derived from the same signal that clocks the digital-to-analog converter.

3. The delitching circuit according to claim 2 wherein latching means are operably disposed between the digital-to-analog converter and the digital input signal.

4. The deglitching circuit according to claim 1 wherein said switch control signal is a delayed version of said clock signal.

5. A deglitching circuit for use on the output signal of a digital-to-analog converter which converts a digital signal to an analog equivalent signal, the deglitching circuit comprising:

switching means having two output terminals, one input terminal, and a control terminal, coupled to receive the output of the digital-to-analog signal, said switching means being switched between said output terminals according to a switch control signal;

delay means coupled to one of said switch output terminals having a delay slightly greater than the width of a typical glitch; and

summing means having two input terminals and one output terminal, the output of said delay means being coupled to one input thereof and the other one of said switch output terminals being coupled to the

other input thereof, said summing means producing a glitch-free analog signal.

6. The deglitching circuit according to claim 5 wherein said switch control signal is derived from the same signal which clocks the digital-to-analog converter.

7. A deglitching circuit substantially as herein described with reference to and as illustrated in the accompanying drawings.

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